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| 10/661,494 | 09/15/2003 | Howard E. Rhodes | M4065.0087/P087-A | 7413 |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>01/28/2008</u>.

2a)☒ This action is **FINAL**.    2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>80-106</u> is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>80-106</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>15 September 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All    b)☐ Some *    c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>9/15/03 & 12/14/07</u>.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments, see page 7, paragraph 2, filed 1/28/2008, with respect to the IDS have been fully considered and are persuasive. The cited references previously crossed out have been considered.

Applicant's arguments, see page 7, paragraph 3, filed 1/28/2008, with respect to claims 80 and 84 have been fully considered and are persuasive. The objections of claims 80 and 84 have been withdrawn.

Applicant's arguments, see page 7, paragraph 4, filed 1/28/2008, with respect to obviousness-type double patenting of claims 80, 81, 83-85, 87-89, and 91 have been fully considered and are persuasive. The obviousness-type double patenting rejections of claims 80, 81, 83-85, 87-89, and 91 have been withdrawn.

Applicant's arguments, (Bird does not have a designated "reset line") with respect to claims 80 and 84 filed 1/28/2008 have been fully considered but they are not persuasive. As essentially admitted by applicant on page 8, paragraph 1 of the remarks, Bird indicates that reference lines 1 and 2 are used for resetting, therefore, regardless of whether Bird calls either reference line (1 or 2) a "reset line" does not change the fact that each one of reference lines (1 and 2) are in fact reset lines which

are used to reset the values of their corresponding pixels (nodes) (10A and 10B) and

therefore both reference lines (1 and 2) read on claimed, **"reset line"**.


Applicant's arguments, (Bird does not indicate the reset line "extends

approximately linearly across the pixel array") with respect to claims 80 and 84 filed

1/28/2008 have been fully considered but they are not persuasive.

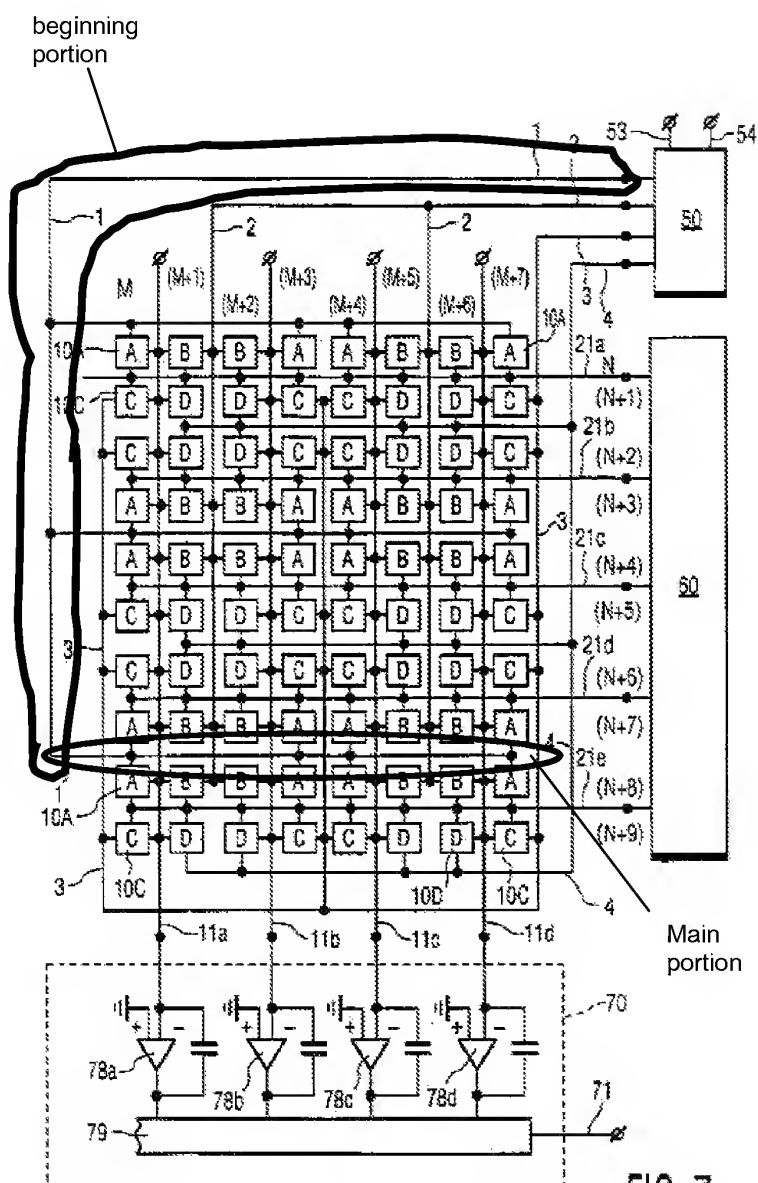beginning
portion

Main
portion

FIG. 7

As clearly shown in figure 7, an expanded version of figure 1, reference line (1)

extends from one end of the array at pixel A to the opposite end of the array at another

pixel A in a straight horizontal line.  The only possible way that reference line (1) can be

interpreted as traveling circuitously is in the beginning portion of the reference line (1)

as labeled above, which travels from voltage pulse generator (50) around to the left side

of the array to where it begins traveling linearly across the array, wherein in that

beginning portion, the reference line (1) is not even traveling **"across"** the array, which

leaves the main portion as labeled above as the only section of the reference line (1)

that travels across the array, wherein the main section is clearly a straight line.  In

addition, even if the reference line is thought to be traveling circuitously as a whole,

because the main portion is part of the reference line (1) and it is linear across the

array, it is enough so that the reference line (1) as a whole is **"approximately"** or

**"substantially"** linear as so broadly claimed.  Similarly, reference line (2) extends

linearly from the top of the array to the bottom of the array and therefore travels

**"approximately linearly across the pixel array"**.


Applicant's arguments (Bird does not disclose "a plurality of odd row select

lines…to address odd pixels in the rows" or "a plurality of even row select lines…to

address even pixels in the rows" or "a row driver to address pixels through the odd row

select lines and the even row select lines") with respect to claim 88 filed 1/28/2008 have

been fully considered but they are not persuasive.  As essentially admitted by applicant

on page 9, paragraph 2 in the remarks, Bird uses single row lines (21a) for all pixels

(10A and 10B) in a row (N), therefore, odd row select lines (21a) address the odd pixels

in the row and the even pixels in the row in addition to the odd pixels.  Regardless of

whether or not Bird discloses the odd row select lines (21a) address *just* the odd pixels

and *not* the even pixels, Bird *does* disclose the **"odd row select lines…address the**

**odd pixels in the rows"**, which is what is claimed.  Similarly, Bird discloses even row

select lines (21b) address the even pixels in the row and the odd pixels in the row in

addition to the odd pixels and therefore **"address even pixels in the rows"**, therefore

the row driver (60) can **"address pixels through the odd row select lines and the**

**even row select lines"**.


Applicant's arguments (Bird fails to disclose limitations relating to the presence

and use of even and odd row select lines, particularly as they are connected to a row

driver) with respect to claim 93 filed 1/28/2008 have been fully considered but they are

not persuasive.  As essentially admitted by applicant on page 9, paragraph 2 in the

remarks, Bird uses single row lines (21a) for all pixels (10A and 10B) in a row (N),

therefore, odd row select lines (21a) address the odd pixels in the row and the even

pixels in the row in addition to the odd pixels.  Regardless of whether or not Bird

discloses the odd row select lines (21a) address *just* the odd pixels and *not* the even

pixels, Bird *does* disclose **"addressing odd pixels in the row of pixels via odd row**

**select line"**, which is what is claimed.  Similarly, Bird discloses even row select lines

(21b) address the even pixels in the row and the odd pixels in the row in addition to the

even pixels and therefore they are capable of **"addressing even pixels in a row of**

**pixels of an array of pixels using a row driver coupled to an even row select line"**,

wherein the row driver (60) is coupled to the even row select lines (21b).

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

*__Claims 80-83, 88-96, 102-104 and 106 are rejected under 35 U.S.C. 102(b) as__*

*__being anticipated by Bird US Patent 5,721,422).__*

Regarding claim 80, Bird discloses electronic devices having an array with

shared column conductors.  In addition, Bird discloses ***"A method of operating an***

***active pixel CMOS imager, comprising:  activating a first pixel in a row connected***

***to a shared column line for a first period of time and then subsequently activating***

***an adjacent second pixel in the row connected to the shared column line for a***

***second period of time, the array comprising the first and second pixels; detecting***

***a first voltage level at a node of the first pixel; resetting the first voltage level of***

***the node to a predetermined voltage using a reset transistor addressed by a reset***

***line that extends approximately linearly across the pixel array; transferring***

***charge collected by the first pixel to the node; detecting the charge at the node;***

***and generating an output signal over the shared column line."***

Specifically, Bird discloses in the time interval A, the –5 volt row pulse is applied

to only the row conductor (21a) of the row N and pixels (10A) and (10B) are connected

to the row conductor (21a) and the reference conductor (1) of pixel (10A) is biased to a

less negative voltage (-2.5V) than the row pulse (-5V) so the rectifying elements (S1)

and (S2) of pixel (10A) are forward biased and so the capacitance of photodiode (8) of

pixel (10A) is recharged and its residual charge read out via the shared column

conductor (11a), which reads on claimed, *"activating a first pixel in a row connected*

*to a shared column line for a first period of time",* as disclosed in column 6 lines 29-

40 and  exhibited in figures 1 and 2 wherein pixel (10A) reads on claimed, *"first pixel."*

In addition, Bird discloses in the time interval B, the row pulse is again applied to row

conductor (21a) of row N, but the reference conductor (1) is at –7.5V so that the

rectifying elements (S1) and (S2) of pixel (10B) are forward-biased so the photodiode

(8) of pixel (10B) is read out and re-charged, which reads on claimed, *"and then*

*subsequently activating an adjacent second pixel in the row connected to the*

*shared column line for a second period of time, the array comprising the first and*

*second pixels",* as disclosed in column 6 lines 40-50 and exhibited in figures 1 and 2,

wherein pixel (10B) reads on claimed, *"second pixel."*

In addition, Bird discloses the capacitance of photodiode (8) of pixel (10A) is

recharged and its residual charge is read out via the shared column conductor (11a),

which reads on claimed, *"detecting a first voltage level at a node of the first pixel",*

as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2, wherein the point

on the column conductor (11a) between the two pixels (10A) and (10B) as shown in

figure 1 reads on claimed, *"node."*

In addition, Bird discloses after the first time interval (A) (when the rectifying

elements (S1) and (S2) of pixel (10A) are forward-biased and the capacitance of

photodiode (8) of pixel (10A) is recharged and read out), the pulse applied to row

conductor (21a) from the row driving circuit (60) is set to 0V and the pulse applied to the

conductor (1) is set to -2.5V. Therefore, the reference conductor (1) is set to a lower

voltage than the row pulse so the rectifying elements (S1) and (S2) are reverse-biased

and therefore set the node between the two photodiodes (8) to a predetermined voltage,

wherein the row pulse is governed by a row driving circuit (60) containing switching of

transistor switches on each row conductor (21) and the reference conductor (1) is

governed by transistor switches (57) and (58), wherein the lines associated with each of

the transistors are extended linearly across the pixel array, which reads on claimed,

***"resetting the first voltage level of the node to a predetermined voltage using a***

***reset transistor addressed by a reset line that extends approximately linearly***

***across the pixel array",*** as disclosed in column 5 lines 30-41 and 50-67 and column 6

lines 13-28 and exhibited in figures 1, 2, and 7, wherein the switching transistors (57)

and (58) read on claimed, *"reset transistor",* and the reference conductors (1, 2, 3,

and 4) read on claimed, *"reset line."* Bird inherently discloses resetting the first

voltage level of the node to a predetermined voltage because every time a sequential

read out of the pixel (10A) is performed the row conductor (21a) is set to –5V and the

reference conductor (1) is set to –7.5V thus turning on the rectifying elements (S1) and

(S2), but when the pixel (10A') is read out, the row conductor (21a) is set to 0V,

therefore at this point, the voltage level of the node is set to a predetermined voltage

governed by the row conductor (21a) being 0V.

In addition, Bird discloses a row pulse is applied to the row conductor (21a) of the

row N including pixel (10A) and when the pulse is –5V the rectifying elements (S1) and

(S2) are forward biased so the capacitance of photodiode (8) of pixel (10A) is recharged

and the charge is read out at the node via the shared column conductor (11a), therefore

the charge is transferred from the photodiode (8) to the node, which reads on claimed,

***"transferring charge collected by the first pixel to the node; detecting the charge***

***at the node; and generating an output signal over the shared column line",*** as

disclosed in column 6 lines 13-30 and exhibited in figures 1 and 2.


Regarding claim 81, Bird discloses everything claimed as applied above (see

claim 1), in addition, Bird discloses ***"The method of claim 80, wherein the shared***

***column line extends approximately linearly across the pixel array."*** Specifically,

Bird discloses the column line (11a) extends linearly from the top of the array to the

bottom of the array, which reads on claimed, ***"the shared column line extends***

***approximately linearly across the pixel array"***, as exhibited in figure 1.


Regarding claim 82, Bird discloses everything claimed as applied above (see

claim 81), in addition, Bird discloses ***"The method of claim 81, further comprising a***

***row select line that extends approximately linearly across the pixel array."***

Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, *"further comprising a row select line that extends approximately linearly across the pixel array"*, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, *"row select line."*

Regarding claim 83, Bird discloses everything claimed as applied above (see claim 80), in addition, Bird discloses *"The method of claim 80, further comprising a row select line that extends approximately linearly across the pixel array."* Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, *"further comprising a row select line that extends approximately linearly across the pixel array"*, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, *"row select line."*

Regarding claim 88, Bird discloses electronic devices having an array with shared column conductors. In addition, Bird discloses *"An active pixel CMOS imager, comprising: a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array; a plurality of column lines each connected to at least two adjacent pixels of a row*

*in the array, the column lines being connected to output circuitry to output the*

*signal; a plurality of odd row select lines orthogonal to the column lines to*

*address odd pixels in the rows; a plurality of even row select lines orthogonal to*

*the column lines to address even pixels in the rows; a column driver to address*

*pixels connected to the column lines; and a row driver to address pixels through*

*the odd row select lines and the even row select lines."*

Specifically, Bird discloses an array of pixels, which reads on claimed*, "plurality*

*of pixels",* as disclosed in column 4 lines 53-55 and exhibited in figure1; wherein the

pixels are read in a known manner by an output circuit (70) and are eventually from an

output (71) to an appropriate store or display wherein each pixel contains a

photosensitive element (8) which store charge in response to light incident on the

element (8) wherein the pixels are arranged in rows and columns of an array, which

reads on claimed, *"to generate an output signal associated with detected light, the*

*plurality of pixels arranged in rows and columns of an array",,* as disclosed in

column 4 lines 64-68 and column 8 lines 15-20 and exhibited in figures 1 and 7.

In addition, Bird discloses a plurality of column lines each connected to at least

two adjacent pixels of a row in the array, the column lines connected to the output circuit

(70) to the output signal (71), which reads on claimed, *"a plurality of column lines*

*each connected to at least two adjacent pixels of a row in the array, the column*

*lines being connected to output circuitry to output the signal",* as exhibited in

figure 7.

In addition, Bird discloses the row conductors (21) are scan lines for scanning the

pixels of the sensor array on a row by row basis and they are orthogonal to the column

lines and address both the odd and even pixels in the rows, which reads on claimed, *"a*

*plurality of odd row select lines orthogonal to the column lines to address odd*

*pixels in the rows",* and claimed, *"a plurality of even row select lines orthogonal to*

*the column lines to address even pixels in the rows",* as disclosed in column 4 lines

55-58 and exhibited in figures 1 and 7, wherein the odd row conductors (21a) read on

claimed, *"odd row select lines"* and the even row conductors (21b) reads on claimed,

*"even row select lines."*

In addition, Bird discloses a column drive circuitry (70) which is used to select the

pixels connected to the column lines, which reads on claimed, *"a column driver to*

*address pixels connected to the column lines",* as disclosed in column 6 lines 59-64

and exhibited in figures 1 and 7.

In addition, Bird discloses a row drive circuit (60) used to scan pixels of the

sensor array on a row by row basis, scanning even and odd rows, which reads on

claimed, *"a row driver to address pixels through the odd row select lines and the*

*even row select lines",* as disclosed in column 4 lines 54-58 and exhibited in figures 1

and 7.


Regarding claim 89, Bird discloses everything claimed as applied above (see

claim 88), in addition, Bird discloses *"The imager of claim 88, wherein the column*

*lines extend approximately linearly across the array."* Specifically, Bird discloses

the column line (11a) extends linearly from the top of the array to the bottom of the array, which reads on claimed, *"the column lines extend approximately linearly across the array"*, as exhibited in figure 1.

Regarding claim 90, Bird discloses everything claimed as applied above (see claim 89), in addition, Bird discloses *"The method of claim 89, wherein the odd and even row select lines extend approximately linearly across the array."* Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, *"the odd and even row select lines extend approximately linearly across the array"*, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-lines read on claimed, *"odd and even row select lines."*

Regarding claim 91, Bird discloses everything claimed as applied above (see claim 88), in addition, Bird discloses *"The method of claim 88, wherein the odd and even row select lines extend approximately linearly across the array."* Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, *"the odd and even row select lines extend approximately linearly across the array"*, as disclosed in column 12 lines 38-

40 and exhibited in figure 1, wherein the scan-lines read on claimed, *"odd and even row select lines."*

Regarding claim 92, Bird discloses everything claimed as applied above (see claim 88), in addition, Bird discloses, *"The imager of claim 88, further comprising a plurality of reset lines that extend approximately linearly across the array."* Specifically, Bird discloses that the reference conductors (1) and (2) are used to reset the pixels after they have been read by reverse-biasing their corresponding rectifying elements (S1) and (S2) using the timing sequence shown in figure 2 wherein the reference conductors (1) and (2) are linear across the array, which reads on claimed, *"a plurality of reset lines that extend approximately linearly across the array"*, as disclosed in column 5 lines 17-40 and exhibited in figure 1 and 2.

Regarding claim 93, Bird discloses a read-out circuit for active matrix imaging arrays.  In addition, Bird discloses *"A method of operating a CMOS imager, comprising:  addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line; providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an even row select line; and providing a second output signal associated with light detected by the odd pixels to the plurality of column lines coupled to the odd pixels."*

Specifically, Bird discloses a row driver circuit (60) is coupled to row conductors (21) and generates pulses using the row conductors (21) as scan lines for scanning the pixels of the sensor array on a row by row basis wherein the scan lines are orthogonal to column lines and address both the odd and even pixels in the rows which reads on claimed, *"addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line",* as disclosed in column 4 lines 55-60 and exhibited in figures 1 and 7, wherein the even row conductors (21b) read on claimed, *"even row select line."*

In addition, Bird discloses the sensing elements (8) are photosensitive diodes which are contained in each pixel (10) wherein the photosensing element (8) is able to store charge in response to light incident on the element (8) wherein the change in charge state of the photodiode (8) at the end of the integration period is read out on the column conductor (11), which reads on claimed, *"providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an even row select line",* as disclosed in column 4 lines 60-65 and column 5 lines 45-50 and exhibited in figures 1 and 7, wherein the change in charge state of the even photodiodes (8) reads on claimed, *"a first output signal."*

In addition, Bird discloses a row driver circuit (60) is coupled to row conductors (21) and generates pulses using the row conductors (21) as scan lines for scanning the pixels of the sensor array on a row by row basis wherein the scan lines are orthogonal to column lines and address both the odd and even pixels in the rows which reads on

claimed, *"addressing odd pixels in a row of pixels via an even row select line"*, as disclosed in column 4 lines 55-60 and exhibited in figures 1 and 7, wherein the even row conductors (21b) read on claimed, *"even row select line."*

In addition, Bird discloses the sensing elements (8) are photosensitive diodes which are contained in each pixel (10) wherein the photosensing element (8) is able to store charge in response to light incident on the element (8) wherein the change in charge state of the photodiode (8) at the end of the integration period is read out on the column conductor (11), which reads on claimed, *"providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an even row select line"*, as disclosed in column 4 lines 60-65 and column 5 lines 45-50 and exhibited in figures 1 and 7, wherein the change in charge state of the odd photodiodes (8) reads on claimed, *"a first output signal."*

Regarding claim 94, Bird discloses everything claimed as applied above (see claim 93), in addition, Bird discloses *"The method of claim 93, wherein the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line."* Specifically, Bird discloses the column lines (11) are linear across the array and orthogonal to the row conductors (21), which reads on claimed, *"the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line"*, as exhibited in figure

1.  Because the row conductors (21) address even and odd pixels the odd row

conductors (21a) read on claimed, *"odd row select line"* and the even row conductors

(21b) reads on claimed, *"even row select line."*


Regarding claim 95, Bird discloses everything claimed as applied above (see

claim 94), in addition, Bird discloses *"The method of claim 94, wherein the odd and*

*even row select lines extend approximately linearly across the array."*  Specifically,

Bird discloses the odd row conductors (21a) and the even row conductors (21b) extend

linearly across the array, which reads on claimed, *"the odd and even row select lines*

*extend approximately linearly across the array"*, as exhibited in figure 1.


Regarding claim 96, Bird discloses everything claimed as applied above (see

claim 94), in addition, Bird discloses *"The method of claim 94, further comprising a*

*plurality of reset lines that extend approximately linearly across the array."*

Specifically, Bird discloses after the first time interval (A) (when the rectifying elements

(S1) and (S2) of pixel (10A) are forward-biased and the capacitance of photodiode (8) of

pixel (10A) is recharged and read out), the pulse applied to row conductor (21a) from

the row driving circuit (60) is set to 0V and the pulse applied to the conductor (1) is set

to -2.5V.  Therefore, the reference conductor (1) is set to a lower voltage than the row

pulse so the rectifying elements (S1) and (S2) are reverse-biased and therefore set the

node between the two photodiodes (8) to a predetermined voltage, wherein the row

pulse is governed by a row driving circuit (60) containing switching of transistor switches

on each row conductor (21) and the reference conductor (1) is governed by transistor

switches (57) and (58), wherein the lines associated with each of the transistors are

extended linearly across the pixel array, which reads on claimed, *"a plurality of reset*

*lines that extend approximately linearly across the array",* as disclosed in column 5

lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7

wherein the reference conductors (1, 2, 3 and 4) read on claimed, *"reset lines."*


Regarding claim 102, Bird discloses a pixel array comprising a row (top row of

figure 7) comprising a plurality of first pixels (odd pixels of the row starting with A on the

left in figure 7) and a plurality of second pixels (the second A from the left and the last A

in the row), which reads on claimed, **"a pixel array comprising a row comprising a**

**plurality of first pixels and a plurality of second pixels"**, as exhibited in figure 7.

In addition, Bird discloses a first row address line (21a) connected to the first

pixels and a second row address line (1) connected with the second pixels, which reads

on claimed, **"a first row address line connected with the first pixels; a second row**

**address line connected with the second pixels"**, as disclosed in column 5 lines 30-

41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7.

Specifically, both the row conductor (21a) and the reference line (1) are used to address

the pixels of the array, and therefore they are both, **"row address line[s]"**.

In addition, Bird discloses a respective column line (11) for each pair of first and

second pixels of the row, which reads on claimed, **"a respective column line for each**

**pair of first and second pixels of the row"**, as exhibited in figure 7.  Specifically,

because there are only two **"second pixels"**, there are only two **"pair[s] of first and second pixels of the row"**, wherein each one ([the second A from the left and the second B from the left] and [the first A from the right and the first B from the right] as in figure 7) has its own column line (11).

In addition, Bird discloses a row conductor (21a) connected to the plurality of first pixels, which reads on claimed, **"a reset line connected to the plurality of first pixels"**, as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7. Specifically, there is no limitation in the claims that requires the first row address line to be a separate entity from the reset line. In addition, the row conductor (21a) is required along with the reference lines (1 and 2) to turn on and off the switches (S1 and S2) and therefore the row conductor (21a) is considered to be a **"reset line"**.

Regarding claim 103, Bird discloses everything claimed as applied above (see claim 102), in addition, Bird discloses the plurality of first pixels are the odd pixels of the row starting from A on the left, which reads on claimed, **"wherein the plurality of first pixels are every other pixel in the row"**, as exhibited in figure 7.

Regarding claim 104, Bird discloses everything claimed as applied above (see claim 102), in addition, Bird discloses wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line (11), which reads on claimed, **"wherein each pair of first and second**

**pixels of the row are arranged with the first and second pixels positioned**

**adjacent each other along the column line",** as exhibited in figure 7.


Regarding claim 106, Bird discloses a row of pixels comprising a first address line (21a) connected to a first plurality of pixels (odd pixels starting from A on the left in figure 7) and a second address line (1) connected to a second plurality of pixels (second A from the left and the last A of the row in figure 7), which reads on claimed, **"a row of pixels comprising a first address line connected to a first plurality of said pixels and a second address line connected to a second plurality of said pixels"**, as exhibited in figure 7.

In addition, Bird discloses a plurality of read-out lines (11b and 11d), each of said read-out lines (11b and 11d) being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels, which reads on claimed, **"a plurality of read-out lines, each of said read-out lines being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels"**, as exhibited in figures 1 and 7.

In addition, Bird discloses a reset line (1) connected to the second plurality of pixels, which reads on claimed, **"a reset line connected to at least the first plurality of pixels or the second plurality of pixels"**, as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

### *Claims 84-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bird in view of Ackland et al. (US Patent 5,576,763) hereinafter referenced as Ackland.*

Regarding claim 84, Bird discloses electronic devices having an array with

shared column conductors.  In addition, Bird discloses in the time interval A, the –5 volt

row pulse is applied to only the row conductor (21a) of the row N and pixels (10A) and

(10B) are connected to the row conductor (21a) and the reference conductor (1) of pixel

(10A) is biased to a less negative voltage (-2.5V) than the row pulse (-5V) so the

rectifying elements (S1) and (S2) of pixel (10A) are forward biased and so the

capacitance of photodiode (8) of pixel (10A) is recharged and its residual charge read

out via the shared column conductor (11a), which reads on claimed, *"activating a first

pixel in a row connected to a shared column line for a first period of time",* as

disclosed in column 6 lines 29-40 and  exhibited in figures 1 and 2 wherein pixel (10A)

reads on claimed, *"first pixel."*  In addition, Bird discloses in the time interval B, the row

pulse is again applied to row conductor (21a) of row N, but the reference conductor (1)

is at –7.5V so that the rectifying elements (S1) and (S2) of pixel (10B) are forward-

biased so the photodiode (8) of pixel (10B) is read out and re-charged, which reads on

claimed, *"and then subsequently activating an adjacent second pixel in the row*

*connected to the shared column line for a second period of time, the array*

*comprising the first and second pixels",* as disclosed in column 6 lines 40-50 and

exhibited in figures 1 and 2, wherein pixel (10B) reads on claimed, *"second pixel."*

In addition, Bird discloses the capacitance of photodiode (8) of pixel (10A) is

recharged and its residual charge is read out via the shared column conductor (11a),

which reads on claimed, *"detecting a first voltage level at a node of the first pixel",*

as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2, wherein the point

on the column conductor (11a) between the two pixels (10A) and (10B) as shown in

figure 1 reads on claimed, *"node."*

In addition, Bird discloses after the first time interval (A) (when the rectifying

elements (S1) and (S2) of pixel (10A) are forward-biased and the capacitance of

photodiode (8) of pixel (10A) is recharged and read out), the pulse applied to row

conductor (21a) from the row driving circuit (60) is set to 0V and the pulse applied to the

conductor (1) is set to -2.5V.  Therefore, the reference conductor (1) is set to a lower

voltage than the row pulse so the rectifying elements (S1) and (S2) are reverse-biased

and therefore set the node between the two photodiodes (8) to a predetermined voltage,

wherein the row pulse is governed by a row driving circuit (60) containing switching of

transistor switches on each row conductor (21) and the reference conductor (1) is

governed by transistor switches (57) and (58), wherein the lines associated with each of

the transistors are extended linearly across the pixel array, which reads on claimed,

***"resetting the first voltage level of the node to a predetermined voltage using a***

***reset transistor addressed by a reset line that extends approximately linearly***

***across the pixel array",*** as disclosed in column 5 lines 30-41 and 50-67 and column 6

lines 13-28 and exhibited in figures 1, 2, and 7, wherein the switching transistors (57)

and (58) read on claimed, ***"reset transistor",*** and the reference conductors (1, 2, 3,

and 4) read on claimed, ***"reset line",*** and Bird inherently discloses resetting the first

voltage level of the node to a predetermined voltage because every time a sequential

read out of the pixel (10A) is performed the row conductor (21a) is set to −5V and the

reference conductor (1) is set to −7.5V thus turning on the rectifying elements (S1) and

(S2), but when the pixel (10A') is read out, the row conductor (21a) is set to 0V,

therefore at this point, the voltage level of the node is set to a predetermined voltage

governed by the row conductor (21a) being 0V.

In addition, Bird discloses a row pulse is applied to the row conductor (21a) of the

row N including pixel (10A) and when the pulse is −5V the rectifying elements (S1) and

(S2) are forward biased so the capacitance of photodiode (8) of pixel (10A) is recharged

and the charge is read out at the node via the shared column conductor (11a), therefore

the charge is transferred from the photodiode (8) to the node, which reads on claimed,

***"transferring charge collected by the first pixel to the node; detecting the charge***

***at the node; and generating an output signal over the shared column line",*** as

disclosed in column 6 lines 13-30 and exhibited in figures 1 and 2.

In addition, Bird discloses the device elements (8) may be photosensitive elements of an image sensor device, wherein the image sensor device has an array of pixels (10), which reads on claimed, *"the imager comprising a pixel array"*, as disclosed in column 4 lines 51-55 and exhibited in figures 1 and 3, however, Bird fails to disclose "*focusing an image on an active pixel CMOS imager"*. However, the examiner maintains that it was well known in the art to provide "*focusing an image on an active pixel CMOS imager"*, as taught by Ackland.

In addition, Ackland discloses a single-polysilicon CMOS active pixel. In addition, Ackland discloses a plurality of single polysilicon active pixels (36) arranged to form an imaging array which may be used as a solid–state camera and in an exemplary imaging array, one or more signal timing controllers may be employed to sequentially activate the pixels in each row generating a serial video signal corresponding to an image focused on the array, which reads on claimed, *"focusing an image on an active pixel CMOS imager",* as disclosed in column 6 lines 61-67.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bird by specifically providing "*focusing an image on an active pixel CMOS imager"*, as taught by Ackland, for the purpose of forming an active pixel using a process wherein only one polysilicon deposition is required, as disclosed in column 1 lines 54-60 and to be used as a solid-state camera as disclosed in column 6 lines 61-67.

Regarding claim 85, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 84), in addition, Bird discloses *"The method of claim 84, wherein the shared column line extends approximately linearly across the pixel array."* Specifically, Bird discloses the column line (11a) extends linearly from the top of the array to the bottom of the array, which reads on claimed, *"the shared column line extends approximately linearly across the pixel array"*, as exhibited in figure 1.

Regarding claim 86, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 81), in addition, Bird discloses *"The method of claim 85, further comprising a row select line that extends approximately linearly across the pixel array."* Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, *"further comprising a row select line that extends approximately linearly across the pixel array"*, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, *"row select line."*

Regarding claim 87, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 80), in addition, Bird discloses *"The method of claim 84, further comprising a row select line that extends approximately linearly across the pixel array."* Specifically, Bird discloses row conductors (21) are scan-lines

for addressing rows of the display elements sequentially on a row by row basis wherein

the row conductors extend linearly across the pixel array, which reads on claimed,

*"further comprising a row select line that extends approximately linearly across*

*the pixel array"*, as disclosed in column 12 lines 38-40 and exhibited in figure 1,

wherein the scan-line reads on claimed, *"row select line."*

## Claims 97-101 and 105 are rejected under 35 U.S.C. 103(a) as being

## unpatentable over Bird in view of Shinohara (US Patent 5,587,738).

Regarding claim 97, Bird discloses a row comprising a first pixel (10a) and a

second pixel (10b), which reads on claimed, **"a row comprising a first pixel and a**

**second pixel"**, as exhibited in figures 1 and 7.

In addition, Bird discloses a column conductor (11a) connected with the first and

second pixels (10a and 10b), which reads on claimed, **"a column line connected with**

**the first and second pixels"**, and, **"the first and second pixels being joined by a**

**[column conducting component]"**, as exhibited in figures 1 and 5-7. However, Bird

fails to specifically disclose that the joining section is **"a diagonal active area"**.

However, the examiner maintains that it was well known in the art to provide that the

joining section is **"a diagonal active area"**, as taught by Shinohara.

In a similar field of endeavor Shinohara discloses a solid-state image pickup

device having plural switches for subtracting a stored signal from a pixel output. In

addition, Shinohara discloses in the Prior art that each of the photosensitive device (P+

diffusion layer 43 and n+ diffusion layer 44) includes an active area for accumulating

photo-generated charge having a diagonal shape component (each pixel is formed so

as to extend toward the middle portion of the adjoining four pixels), which reads on

claimed, **"a diagonal active area"**, as disclosed in column 1 line 55 through column 2

line 12 and exhibited in figure.

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to apply the technique of using **"a diagonal active area"**,

as taught by Shinohara, to achieve the predictable result of connecting two storage

nodes together so that they share a common column line as shown in figures 1, 4, and

7 of Bird for the purpose of more efficiently resetting all pixels in a selected row line

simultaneously and improve performance.

In addition, Bird discloses an even row line (21a) connected with the first pixel

(10a) and an odd row line (21a) connected with the second pixel (10b), which reads on

claimed, **"an even row line connected with the first pixel; an odd row line**

**connected with the second pixel"**, as exhibited in figures 1 and 7. Specifically, the

even row line and odd row line are not limited to two separate entities by the claim

language and therefore the row conductor (21a) reads on claimed, **"an even row line"**,

and it also reads on claimed, **"an odd row line"**.


Regarding claim 98, Bird discloses everything claimed as applied above (see

claim 97), in addition, Bird discloses the row comprises a plurality of first pixels (A) and

a plurality of second pixels (B), which reads on claimed, **"wherein the row further**

comprises a plurality of first pixels and a plurality of second pixels", as exhibited in figure 7.

Regarding claim 99, Bird discloses everything claimed as applied above (see claim 97), in addition, Bird discloses the row conductor (21a) extends linearly across an array of pixels, which reads on claimed, "wherein the even row line and the odd row line extends substantially linearly across an array of pixels", as exhibited in figures 1 and 5-7.

Regarding claim 100, Bird discloses everything claimed as applied above (see claim 97), in addition, Bird discloses a first reset line (1) for the first pixel (A) and a second reset line (2) for the second pixel (B), which reads on claimed, "a first reset line for the first pixel and a second reset line for the second pixel", as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7.

Regarding claim 101, Bird discloses everything claimed as applied above (see claim 100), in addition, Bird discloses each of the row conductor (21a), the first reset line (1), and the second reset line (2) extend substantially linearly across the first and second pixels (A and B), which reads on claimed, "wherein each of the even row line, odd row line, first reset line, and second reset line extend substantially linearly across the first and second pixels", as exhibited in figures 1 and 5-7.

Regarding claim 105, Bird discloses everything claimed as applied above (see claim 102), in addition, Bird discloses each pair of first and second pixels are connected through a common column line (11), which reads on claimed, **"the first and second pixels are connected by a [column conducting component]"**, as exhibited in figures 1 and 5-7.  However, Bird fails to specifically disclose that the joining section is **"a substantially diagonal active area"**.  However, the examiner maintains that it was well known in the art to provide that the connection is **"a substantially diagonal active area"**, as taught by Shinohara.

In a similar field of endeavor Shinohara discloses a solid-state image pickup device having plural switches for subtracting a stored signal from a pixel output.  In addition, Shinohara discloses in the Prior art that each of the photosensitive device (P+ diffusion layer 43 and n+ diffusion layer 44) includes an active area for accumulating photo-generated charge having a diagonal shape component (each pixel is formed so as to extend toward the middle portion of the adjoining four pixels), which reads on claimed, **"a substantially diagonal active area"**, as disclosed in column 1 line 55 through column 2 line 12 and exhibited in figure.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of using **"a substantially diagonal active area"**, as taught by Shinohara, to achieve the predictable result of connecting two storage nodes together so that they share a common column line as shown in

figures 1, 4, and 7 of Bird for the purpose of more efficiently resetting all pixels in a

selected row line simultaneously and improve performance.


### *Conclusion*

**THIS ACTION IS MADE FINAL.**  Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action.  In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action.  In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to PAUL BERARDESCA whose telephone number is

(571)270-3579.  The examiner can normally be reached on Mon- Fri 7:30am-5:00pm

EST (Alternate Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ngoc Yen Vu can be reached on (571)272-7320.  The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system.  Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Paul  Berardesca
Examiner
Art Unit 2622


PB
April 22, 2008


*/Ngoc-Yen T. VU/*
*Supervisory Patent Examiner, Art Unit 2622*